a plurality of computing units operating in parallel according to the plurality of instruction codes held in said instruction code holding means;

an access port register file being shared by said plurality of computing devices, each of said plurality of computing devices reading/writing a content of said register file through a corresponding access port for computation; and

a plurality of data memory banks each operated with at least one of said computing devices having means for issuing an instruction to load/store data to/from said access port register file, independently from other data memory banks.

B'

2. (Amended) A processor comprising:

a memory for storing an instruction code and data;

an instruction code holding means for holding a plurality of instruction codes read from said memory; and

a plurality of computing units operating in parallel according to the plurality of instruction codes held in said instruction code holding means;

an access port register file being shared by said plurality of computing devices, each of said plurality of computing devices reading/writing a content of said register file through a corresponding access port for computation; and

a plurality of data memory banks each operated with at least one of said computing devices having means for issuing an instruction to load/store data to/from said access port register file,